ADAPTIVE MOSFET RESISTOR

BACKGROUND OF THE INVENTION

Field of the Invention: This invention relates bipolar- junction transistor (BJT) /MOSFET integrated circuit, particularly to resistive means to bias a BJT with a MOSFET.

Brief Description of Related Art: In integrated circuits, a polycrystalline film or diffusion is often used to fabricate resistors. Such resistors are limited in range of resistance values and may occupy substantial areas. Although it is well-known that a MOSFET can operate as a resistor in its ohmic or "triode" region of its drain V-I characteristics, it is seldom used in practice, because the resistance value varies with the gate voltage.

In circuit applications, a resistor is used to determine the current flow across a voltage differential, for instance between the supply voltage and an electrode of a transistor. For a BJT common emitter amplifier as shown in Fig.1a, once the dc collector current I_{C1} is chosen, the dc base current I_B must be $1/\beta$ times less. Normally, the value of beta varies over a wide range in any production line, and if I_B is fed from a positive power supply through a resistor R_B to the base of an NPN transistor, the resistance value must vary accordingly. Besides, the base resistance value may be too low to shunt the input signal Vin coupled to the base. If the collector is fed through an inductive load, there is no dc voltage drop the load and the minimum required Vcc is the sum of dc base-to-emitter voltage V_{BE} and the drop across the R_B.

If the dc base current is supply from a current mirror as shown in Fig.1b, the effective beta is reduced, and the input resistance is further reduced to shunt the input signal Vin.

In another instance as shown in Fig.1c, it is desired to operate Q1 at a specified collector current I_{C1}. Then the base current I_B should be equal I_{C1}/β. This base current can be derived from the reference base current of Q3 through current mirrors Q2,Q2', where Q3 is fed from a current source with current mirror Q4, Q4'. A current mirror usually has a master section e.g. Q2' and Q4' and a slave section e.g. Q2 and Q4. The dc collector- to-emitter voltage of the master section with the base shorted to the collector must be equal to the turn-on voltage of the BJT, typically in the 0.7V-0.8 V range. The dc collector-to-emitter voltage of the slave section need not be as large, so long as the BJT operates in the active region typically >0.1-0.2V. The dc supply voltage must at least allow enough headroom V_{CE4} (<0.2V) for the current source Q4, the base-to-emitter voltage V_{BE3} (>0.7V) of the reference BJT Q3 and the base-to-emitter voltage $V_{CE2'}$ (>0.7) of the current mirror Q2' for a total of more than 1.5 V. For a standard battery, the rated voltage is 1.5 V new, and for a mercury

cell, the voltage is only 1.3V new. For low voltage application, it is desirable to operate the circuit below 1.3V. Thus the circuit shown in Fig.1c needs at least a supply voltage V_{CC} higher than $V_{CE4}(>0.2V)+V_{BE3}(>0.7V)+V_{CE2}(>0.7V) >1.6V$, which is not suitable for single battery low voltage operation.

SUMMARY OF THE INVENTION

It is proposed here to use an adaptive gate MOSFET to serve as an ohmic resistor by operating the MOSFET is the linear region of the drain characteristics. The proposed adaptive gate MOSFET is to achieve the following objects:

- to adapt to a wide range of resistance value for any specified current and voltage drop;
- to require lower voltage drop than a current mirror, hence low supply voltage;
- to mirror the resistance to more than one resistance values;
- to float the gate of the MOSFET to adapt to the voltage across the resistor and the current through the resistor;
- to reduce the area occupied by the resistors in an IC.

These objects are achieved by using a MOSFET operating in the ohmic region of the drain V-I characteristic to bias the base of a BJT. The gate voltage of the MOSFET is adaptable, so the MOSFET resistor feeds the correct amount of dc base current to yield a desired dc collector current over a wide range of current amplification factor β. The adaptive gate voltage can be obtained by deriving the gate voltage from a current regulator or simply floating the gate.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1a,b,c show prior art means for biasing a BJT common-emitter amplifier.

Fig.2a shows a MOSFET serving as a base biasing resistor for a pnp transistor; Fig.2b shows the operating point of the MOSFET resistor; Fig.3c shows a MOSFET resistor biasing a pnp current mirror for feeding a base current to an npn common emitter amplifier.

Fig 3 shows a base current regulating circuit for deriving an adaptable gate voltage to the MOSFET resistor to bias the base of a BJT.

Fig.4a shows a MOSFET resistor for biasing the base of a BJT differential pair; Fig.4b shows two MOSFET resistor for biasing two bases of a BJT differential pair.

Fig. 5a shows common source and common gate MOSFET resistor mirrors; Fig.5b shows channel stops for the structure of Fig.5a.

DETAILED DESCRIPTION OF THE INVENTION

Operation of the MOSFET Resistor:

Fig.2a shows the use of a n-channel MOSFET Mn as a base resistor for biasing a pnp BJT Qp of a common emitter amplifier. The dc drain characteristic is shown in Fig.2b. The current I_D of a MOSFET is given as:

$$I_D = kp(W/L)\,[(V_{GS}-Vt)\,V_{DS} - V_{DS}^2/2] \qquad (1)$$

where kp is a transconductance parameter, W/L is the width-to-length ratio of the gate, V_{GS} is the gate to source voltage, Vt is the threshold voltage and V_{DS} is drain-to-source voltage. When V_{DS} is less than $(V_{GS}-Vt)$, the MOSFET is operating in the ohmic region, and

$$I_C \approx kp(W/L)\,(V_{GS}-Vt)\,V_{DS} \qquad (2)$$

The ohmic resistance is:

$$R_{DS} = V_{DS}/I_C = 1/[kp(V_{GS}-Vt)] \qquad (3)$$

By adjusting V_{GS}, a wide range of resistance values can be obtained, so long as V_{DS} is less than $(V_{GS}-Vt)$.

Fig.2c shows the use of Qp' similar to the pnp amplifier shown in Fig.2a as the master section of a current mirror fed from the MOSFET resistor Mn. The slave section Qp mirrors the current through Mn to the master section Qp'. The gate voltage V_G is adjusted to flow in Mn a current equal to $1/\beta$ that of the desired I_C for Q1. As compared to Fig.1c, Fig.2c has one less V_{BE3}~0.7V headroom in Q3 and the supply voltage can be as low as the sum of $V_{BE1}+V_{CE2knee}$ <1V, where the voltage drop across Mn can be as low as the knee voltage of Q2.

Design of the Adaptive MOSFET Resistor:

Consider the pnp common emitter circuit Fig.2a with the base of Qp' fed from a nMOS resistor Mn with a gate voltage V_G. The operating point of Mn is shown in Fig.2b. The supply voltage $V_{CC} = (V_{BE} + V_B)$. For common emitter npn amplifier Q1 as shown in Fig.2c, the base is preferably fed from a current source Qp operating in the active region (i.e. above the knee V_{knee} of the collector characteristic ~ 0.15V). Thus the minimum supply voltage $V_{CC} = (V_{BE} + V_{knee}) = 0.8 + 0.15 =$ 0.95V. When the current source Qp is mirrored from a master pnp Qp', the operation of Qp' is similar to that in Figs. 2a with V_B=0.15V. For the ohmic operation of the MOSFET resistor shown in Fig.2a, the dc voltage across of the MOSFET should operate at a V_{DS} less than the knee voltage, i.e.

$$V_B=(V_{CC}-V_{BE\cdot})<(V_G-Vt) \qquad (4)$$

or

$$(V_{CC} - V_{BE} + Vt) < V_G \qquad (5)$$

Since $V_{CC} > V_G$ (6)

Combining (5) and (6) yields:

$$V_{BE} > Vt \quad (7)$$

For $I_B > 0$, $V_B > 0$, as shown in Fig. 2b. For The minimum V_B can be obtained from the following consideration: Since the base of the BJT is the signal input terminal of a common emitter amplifier, the base should preferably be fed from a high impedance current source as shown in Fig.2c, instead of the low ohmic resistance of MOSFET to avoid shunting the signal. The minimum voltage across a current source Qp should be higher that the saturation voltage Vsat, typically ~0.15V. Thus, the minimum supply voltage is:

$$V_{CC} > (V_{BE} + Vsat) = 0.8 + 0.15 = 0.95V$$

The current source Qp is mirrored from the master BJT Qp', which is fed from an adaptable MOSFET resistor Mn described above.

The size of the MOSFET resistance can be calculated as follows:

$$I_B = I_C/\beta = I_D = kp(W/L)\,(V_{CC}-V_G-Vt)(V_{CC}-V_B) \quad (8)$$

$$W/L = (I_C/\beta) / [kp(V_{CC}-V_G-Vt)(V_{CC}-V_B)] \quad (9)$$

A medium value of gate voltage can be derived from Eq. (5),

$$V_G = (V_{CC} - V_B)/2 \quad (10)$$

This medium V_G can allow a I_C/β variation twice that of the medium value.

Derivation of the Gate Voltage:

The gate voltage for the MOSFET resistor can be obtained as follows: The gate voltage can be derived with a regulator circuit as shown in Fig.3. Consider a complementary circuit of Fig.2a, where a pMOS Mp' is used to drive the base of an npn BJT Q1', which is identical to Q1 in Figs.1a-c. The MOSFET Mp' corresponding R_B in Fig.1a is connected between supply V_{CC} and the base of BJT Q1' corresponding to Q1. The collector of Q1' is connected to a current mirror Q5, Q5', which mirrors the collector current of Q1'. The mirror current out of Q5 is compared with the desired collector current for Q1 as a reference current Iref from a current mirror Q6,Q6'. An error voltage V_G is developed and applied to the gate of Mp'. The feedback loop regulates the base current Q1' to yield the desired reference emitter current Iref. Then V_G is the adaptive gate voltage.

Floating Gate Operation:

When the voltage across the MOSFET resistor and the current are known, there is only one gate voltage for the MOSFET resistor to satisfy this condition. Thus, if the voltage across the MOSFET is

given and the current is given, the gate automatically adjusts itself, even if it is floating. This feature can sometimes be utilized as illustrated in Figs. 4a,4b. When the gate of the MOSFET is floating, and V_{DS} and I_C are given, then V_{GS} must assume a value to satisfy Eq. (3). Therefore, the resistance value is adaptive.

A circuit to demonstrate this floating gate resistor is shown in Fig.4a. An npn differential pair Q7, Q8 is fed from a current source Io. The base of Q8 is fixed at dc voltage V_{Ref}. For balanced operation, the dc base voltage of Q7 must be equal to that of Q8, i.e. V_{Ref}, and the dc base currents I_{B7} and I_{B8} must be equal to $Io/2(1+\beta)$. Since the dc base current I_{B7} and the dc base voltage are known, the base of Q6 can be fed from a floating gate MOSFET M7 as a resistor. The floating gate of M7 automatically assumes a resistance value for the appropriate base current for Q7.

This resistance can be duplicated (mirrored) in other resistors on the same chip. For instance in Fig.4b, there is another differential pair Q7', Q8' similar to Q7, Q8 in Fig.4a, fed from a similar current source Io. The base biasing resistors can be duplicated by two MOSFET resistors M7', M8' identical to M7. If the current source is different from Io, say 2Io, In such a case, the resistance M8' feeding the base should be doubled. This can be done by doubling the W/L ratio of M8' as compared the W/L ratio of M8. For the differential pairs in Figs.4a, 4b, one more headroom for Q9 than that in Fig.2c is required, i.e. $V_{CE9} + 1.0V < 1.2V$

If the values of the MOSFET resistors shown in Figs.4a,4c are too low to shunt the input signals, the techniques shown in Fig.2c can be used.

To simulate the floating MOSFET, a dc gate voltage must be assigned to the floating gate. In a typical simulation program such as SPICE, the program does not run with the gate floating. The floating gate voltage can be derived from the regulated gate voltage derived from Fig.3.

Layout of the Floating Gate Resistor:

The floating gate MOSFETs such as M7, M8' can share a common source and a common floating gate, but different drains D7, D7', D8'. A layout is shown in Fig.5a. Such a layout can save area. To prevent cross-talks among the different floating gate MOSFETs, the different MOSFETs can be separated to each other by channel stops shown in dotted lines in Fig.5b as is well known in the IC art. The floating gate should be sealed in oxide and not connected to any parts of the circuit to prevent leakage.

In the foregoing descriptions of the current mirrors in Figs. 1c, 2c,3, 4a and 4b, it is implied that the currents in the master sections are the same as that in the slave sections. However, the currents in

the master sections can be reduced by reducing the emitter sizes of the master sections as is well known in the current mirror art. Also, the BJT current mirrors in these circuits can be replaced with corresponding MOSFETs, i.e pMOS for pnp BJTs and nMOS for npn BJTs.

While the preferred embodiments of the invention have been described, it will be apparent to those skilled in the art that various modifications can be made without departing the spirit of the present invention. Such modifications are all within the scope of the present invention.